REMARKS

Claims 1-34 are pending in the Application. The Office Action dated April 16, 2003 rejected claims 1-34 under 35 U.S.C. §102 as being anticipated by Dorinski (U.S. Patent No. 5,001,038).

By this response, Claims 1, 8, 15, 20, 32, 33 and 34 have been amended to further differentiate the subject matters of the amended claims from the teaching of Dorinski. Claims 5 and 27 are cancelled. Claims 1-34 remain pending. Reconsideration of the application is respectfully requested.

Rejection under 35 USC §102

In the Office Action, claims 1-34 were rejected under 35 U.S.C. 102(b) as being anticipated by Dorinski. The Examiner asserts that the Dorinski reference discloses each of the recited features of all the claims (including all independent claims) of the invention.

In response to the rejection of the above claims, the applicant respectfully submits that Dorinski does not anticipate the applicant's invention according to the independent claims, especially as amended.

Dorinski discloses a process for manufacturing a three-dimensional printed circuit substrate using a planar mask and image projection photolithography. In one of the photolithography process, the substrate is positioned at a first position and a first printed circuit image of a first mask is focused onto a first plane, thereby forming the first printed circuit image on the substrate surface. A second mask having a second printed circuit pattern is substituted for the first mask and the substrate is moved to a second position such that the second printed circuit image is focused on a second plane.

The claimed invention (claims 1, 8, 20, 33 and 34) discloses a structuring method which includes exposing a pattern onto a substrate surface using photolithography. The photolithography process includes a first exposure step for focusing a first pattern onto a first focal plane and a second

exposure step for focusing a second pattern onto a second focal plane. The first pattern portion and the second pattern portion are exposed in a manner so that the two portions overlap partly on the substrate surface.

The Examiner is of the opinion that col 5 line 61-68, col 6 lines 1-14 and Figure 6 of Dorinski discloses that the first and second pattern portions overlap each other. The applicant respectfully disagrees with the Examiner. Specifically, Dorinski teaches that the two printed circuit images (or pattern portions) **604A and 604B** have complementary images, and hence non-overlapping, with the first image forming the lower half and the second image forming the upper half of the overall printed circuit pattern. (See Dorinski, Figure 6, attached Exhibit A.) Also, Figure 6 of Dorinski does not show an overlapping pattern portions on the substrate surface. Therefore, the applicant submits that Dorinski does not teach that the first and second printed circuit images overlap each other according to the claimed invention.

The applicant submits that for anticipation under §102, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. The anticipation requires identity in the claimed features of the claims. Such is not the case between the applicant's claimed invention and Dorinski's teachings as discussed above.

In view of the foregoing, it is respectfully submitted that the applicant's invention according to the amended Claims 1, 8, 20, 33 and 34 are clearly distinguished from what is disclosed by Dorinski and thus is allowable under 35 U.S.C. §102 over Dorinski.

With respect to the dependent claims 2-7, 8-19 and 21-32, the applicant submits that these claims are also allowable in that they variously depend from either claim 1, 8 or 20.

The applicant would also like to point out respectfully that the overlapping of the first and second pattern portions on the substrate surface ensures a reliable exposure of the pattern in the case of a slight misalignment. When such an overlapping of the first and second pattern portions is not

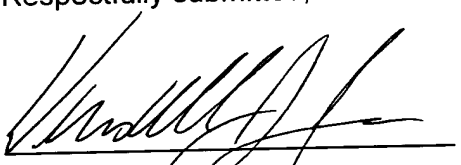
provided, as in the case of Dorinski, a slight misalignment of the first and second pattern portions may cause the image projected on the substrate to be disjointed. This will adversely affect the subsequent process steps of the substrate.

The feature of overlapping the first and second pattern portions on the substrate surface according to the invention is thus advantageous, and is not suggested nor hinted by the teaching of Dorinski.

In view of the discussions set forth herein, it is respectfully submitted that the grounds for the Examiner's rejections have been overcome. Accordingly, it is respectfully submitted that Claims 1-4, 6-26, 28-34 as amended should be found to be in condition for allowance.

Date: August 21, 2003

Respectfully submitted,



Wendell J. Jones
Attorney for Applicant
Reg. No.: 45,961
Telephone No.: (650) 857-7453

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400